MC74AC573, MC74ACT573

Octal Buffer/Line Driver with 3-State Outputs

The MC74AC573/74ACT573 is a high−speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

The MC74AC573/74ACT573 is functionally identical to the MC74AC373/74ACT373 but has inputs and outputs on opposite sides.

Features

- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to MC74AC373/74ACT373
- 3−State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- ′ACT573 Has TTL Compatible Inputs
- Pb−Free Packages are Available*

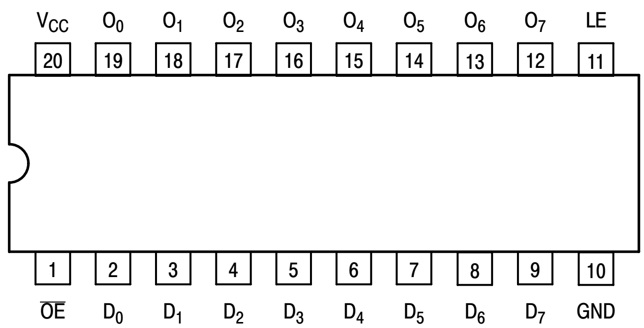


Figure 1. Pinout 20−Lead Packages Conductors
(Top View)

PIN ASSIGNMENT

PIN	FUNCTION
D_0−D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	3−State Output Enable Input
O_0−O_7	3−State Latch Outputs

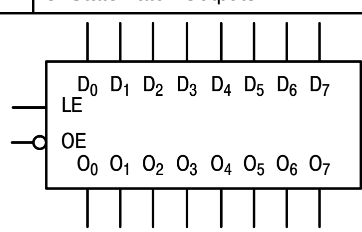


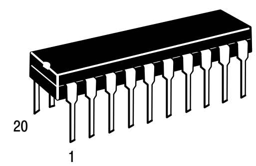
Figure 2. Logic Symbol

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

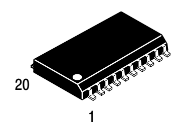
http://onsemi.com

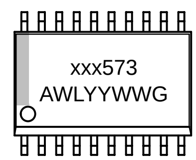
MARKING DIAGRAM



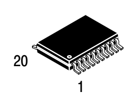


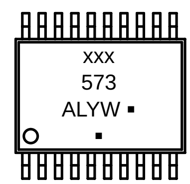
PDIP−20
N SUFFIX
CASE 738



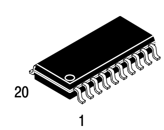


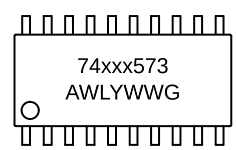
SO−20
DW SUFFIX
CASE 751D





TSSOP−20
DT SUFFIX
CASE 948E





EIAJ−20
M SUFFIX
CASE 967

xxx = AC or ACT
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

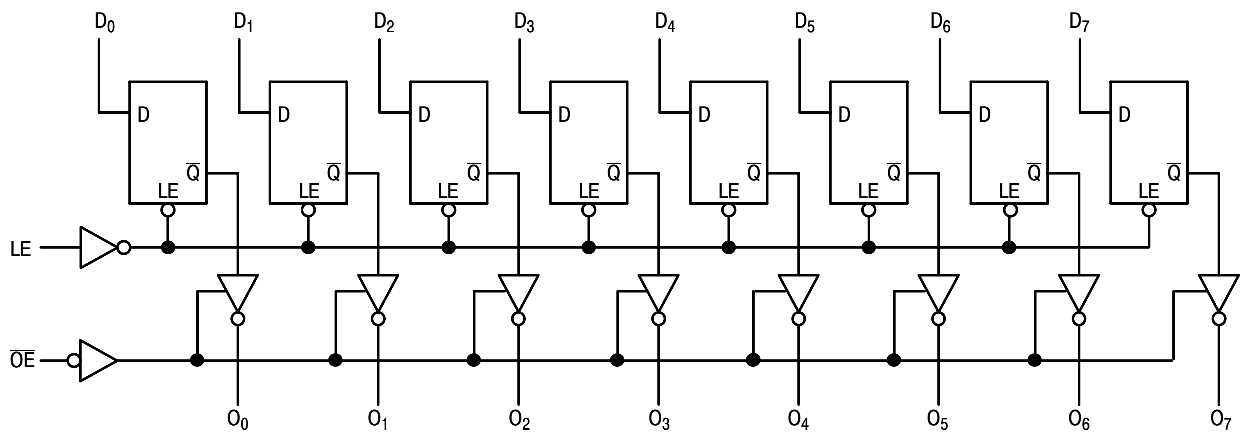
TRUTH TABLE

Inputs			Outputs
OE	**LE**	**D_n**	**O_n**
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before LOW−to−HIGH Transition of Clock

Functional Description

The MC74AC573/74ACT574 contains eight D−type latches with 3−state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH−to−LOW transition of LE. The 3−state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.



NOTE: That this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)		0	−	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	−	150	−	ns/V
		V_{CC} @ 4.5 V	−	40	−	
		V_{CC} @ 5.5 V	−	25	−	
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	−	10	−	ns/V
		V_{CC} @ 5.5 V	−	8.0	−	
T_J	Junction Temperature (PDIP)		−	−	140	°C
T_A	Operating Ambient Temperature Range		−40	25	85	°C
I_{OH}	Output Current − High		−	−	−24	mA
I_{OL}	Output Current − Low		−	−	24	mA

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC T_A = +25°C Typ	74AC T_A = +25°C Guaranteed Limits	74AC T_A = −40°C to +85°C Guaranteed Limits	Unit	Conditions
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I_{OUT} = −50 µA
		3.0 4.5 5.5	− − −	2.56 3.86 4.86	2.46 3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} −12 mA I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I_{OUT} = 50 µA
		3.0 4.5 5.5	− − −	0.36 0.36 0.36	0.44 0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	−	±0.1	±1.0	µA	V_I = V_{CC}, GND
I_{OZ}	Maximum 3−State Current	5.5	−	±0.5	±5.0	µA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	−	−	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	−	−	−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	−	8.0	80	µA	V_{IN} = V_{CC} or GND

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.
*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF			74AC T_A = −40°C to +85°C C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3 5.0	2.5 2.5	− −	13.0 10.0	2.0 2.0	15.0 11.5	ns	3−5
t_{PHL}	Propagation Delay D_n to O_n	3.3 5.0	2.5 2.5	− −	12.0 9.5	2.0 2.0	14.0 11.0	ns	3−5
t_{PLH}	Propagation Delay LE to O_n	3.3 5.0	2.5 2.5	− −	13.0 9.5	2.0 2.0	15.0 11.0	ns	3−6
t_{PHL}	Propagation Delay LE to O_n	3.3 5.0	2.5 2.5	− −	12.0 8.5	2.0 2.0	14.0 10.0	ns	3−6
t_{PZH}	Output Enable Time	3.3 5.0	2.5 2.5	− −	11.0 9.0	2.0 2.0	12.0 10.0	ns	3−7
t_{PZL}	Output Enable Time	3.3 5.0	2.5 2.5	− −	11.0 8.5	2.0 2.0	12.5 9.5	ns	3−8
t_{PHZ}	Output Disable Time	3.3 5.0	2.5 2.5	− −	12.5 11.0	2.0 2.0	13.5 12.0	ns	3−7
t_{PLZ}	Output Disable Time	3.3 5.0	2.5 2.5	− −	9.5 8.0	2.0 2.0	10.5 9.0	ns	3−8

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C C_L = 50 pF		74AC T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	− −	3.5 3.0	4.0 3.5	ns	3−9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	− −	2.0 2.0	2.0 2.0	ns	3−9
t_w	LE Pulse Width, HIGH	3.3 5.0	− −	6.0 4.0	7.0 5.0	ns	3−6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT $T_A = +25°C$ Typ	74ACT $T_A = +25°C$ Guaranteed Limits	74ACT $T_A = -40°C$ to $+85°C$ Guaranteed Limits	Unit	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5	− −	3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5	− −	0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	−	±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6	−	1.5	mA	V_I = V_{CC} − 2.1 V
I_{OZ}	Maximum 3-State Current	5.5	−	±0.5	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	−	−	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	−	−	−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	−	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF Min	Typ	Max	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Min	Max	Unit	Fig. No.
t_{PLH}	Propagation Delay D_n to O_n	5.0	2.5	−	10.5	2.0	12	ns	3−5
t_{PHL}	Propagation Delay D_n to O_n	5.0	2.5	−	10.5	2.0	12	ns	3−5
t_{PLH}	Propagation Delay LE to O_n	5.0	3.0	−	10.5	2.5	12	ns	3−6
t_{PHL}	Propagation Delay LE to O_n	5.0	2.5	−	9.5	2.0	10.5	ns	3−6
t_{PZH}	Output Enable Time	5.0	2.0	−	10	1.5	11	ns	3−7
t_{PZL}	Output Enable Time	5.0	1.5	−	9.5	1.5	10.5	ns	3−8
t_{PHZ}	Output Disable Time	5.0	2.5	−	11	1.5	12.5	ns	3−7
t_{PLZ}	Output Disable Time	5.0	1.5	−	8.5	1.0	9.5	ns	3−8

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF		74ACT T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	−	3.0	3.5	ns	3−9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−	0	0	ns	3−9
t_w	LE Pulse Width, HIGH	5.0	−	3.5	4.0	ns	3−6

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	25	pF	V_{CC} = 5.0 V

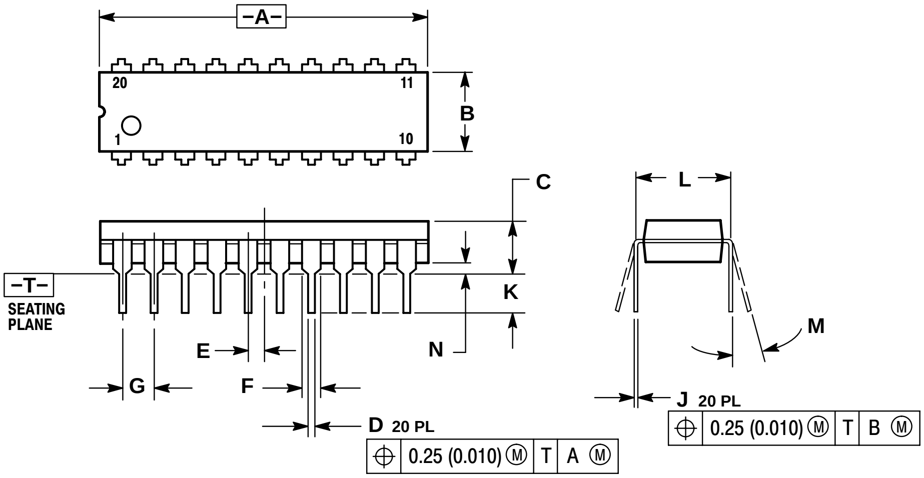
ORDERING INFORMATION

Device	Package	Shipping†
MC74AC573N	PDIP−20	18 Units / Rail
MC74AC573NG	PDIP−20 (Pb−Free)	18 Units / Rail
MC74AC573DW	SOIC−20	38 Units / Rail
MC74AC573DWG	SOIC−20 (Pb−Free)	38 Units / Rail
MC74AC573DWR2	SOIC−20	1000 Units / Tape & Reel
MC74AC573DWR2G	SOIC−20 (Pb−Free)	1000 Units / Tape & Reel
MC74AC573DTR2	TSSOP−20*	2500 Units / Tape & Reel
MC74AC573DTR2G	TSSOP−20*	2500 Units / Tape & Reel
MC74AC573MEL	SOEIAJ−20	2000 Units / Tape & Reel
MC74AC573MELG	SOEIAJ−20 (Pb−Free)	2000 Units / Tape & Reel
MC74ACT573N	PDIP−20	18 Units / Rail
MC74ACT573NG	PDIP−20 (Pb−Free)	18 Units / Rail
MC74ACT573DW	SOIC−20	38 Units / Rail
MC74ACT573DWG	SOIC−20 (Pb−Free)	38 Units / Rail
MC74ACT573DWR2	SOIC−20	1000 Units / Tape & Reel
MC74ACT573DWR2G	SOIC−20 (Pb−Free)	1000 Units / Tape & Reel
MC74ACT573DTR2	TSSOP−20*	2500 Units / Tape & Reel
MC74ACT573DTR2G	TSSOP−20*	2500 Units / Tape & Reel

†For information on tape and reel specifications,including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This package is inherently Pb−Free.

PACKAGE DIMENSIONS

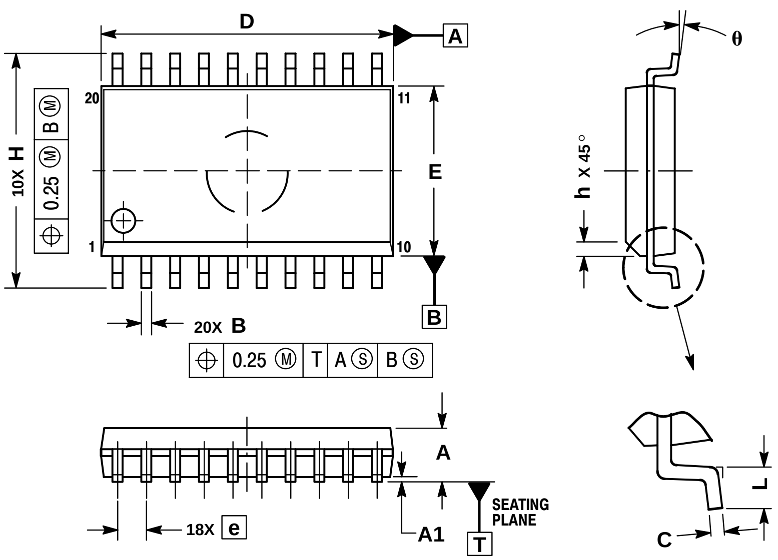
PDIP−20
N SUFFIX
20 PIN PLASTIC DIP PACKAGE
CASE 738−03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

SO−20
DW SUFFIX
20 PIN PLASTIC SOIC PACKAGE
CASE 751D−05
ISSUE G

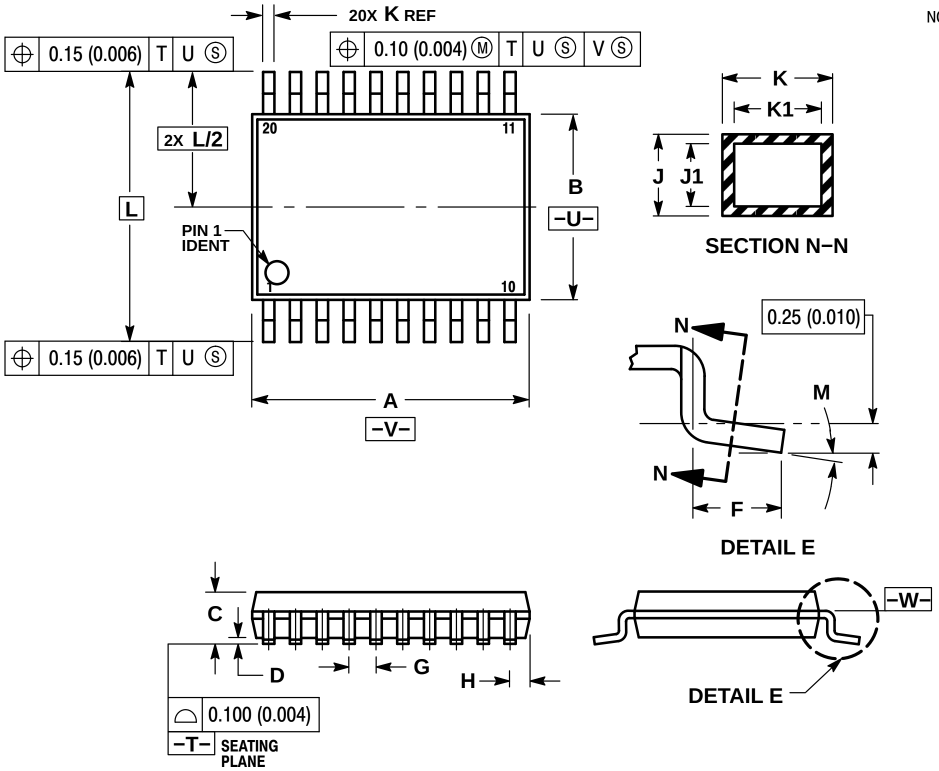


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

PACKAGE DIMENSIONS

TSSOP−20
DT SUFFIX
20 PIN PLASTIC TSSOP PACKAGE
CASE 948E−02
ISSUE B

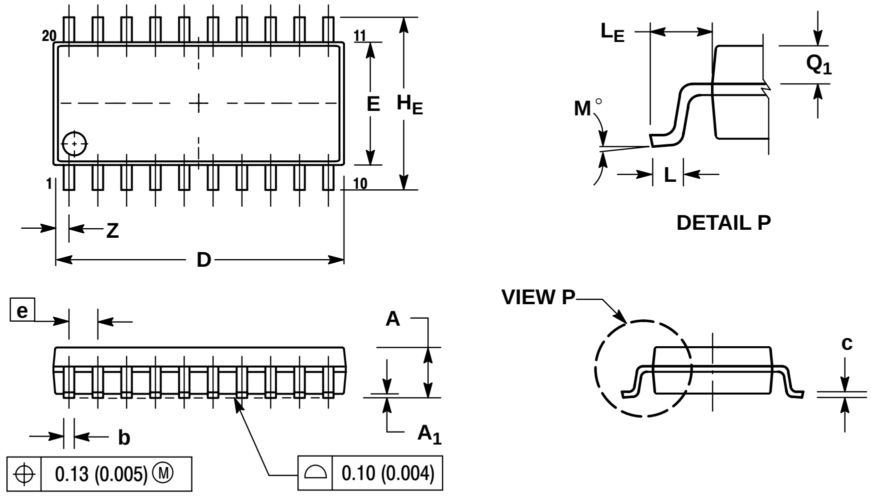


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

PACKAGE DIMENSIONS

SOEIAJ−20
M SUFFIX
20 PIN PLASTIC EIAJ PACKAGE
CASE 967−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

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